

# **APPLICATION NOTE**

**TDA8761A / TDA8763 / TDA8763A**  
**Evaluation board documentation**

**AN/96028**



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## **APPLICATION NOTE**

### **TDA8761A / TDA8763 / TDA8763A Evaluation board documentation**

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## Summary

This note describes a demonstration board which facilitates the evaluation of the TDA8763(A) 10 bit analog to digital converters and the TDA8761A 9 bit analog to digital converter (sections 2, 3, 4, 10, 11).

In addition the functioning of the TDA8763(A) is shortly described (sections 1, 5, 7, 8) and several methods to provide input offset and top and bottom references are shown (sections 5, 6).

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**AN/96028****1. INTRODUCTION**

TDA8761A, TDA8763 and TDA8763A are high speed, low power, pin to pin compatible, analog to digital converters.

They have been designed for professional applications: video data digitizing, medical imaging,  $\Sigma\Delta$  modulators, cable TV, Digital Video Broadcasting (DVB)...

Main features of these ADCs, which are derived from the same ADC core, are shown in the following table:

	Resolution (bit)	Full Scale Bandwidth (MHz)	Power (mW)	Sampling Frequency (MSPS)	Built-in voltage regulator	outputs directly compatible with low voltage logic
TDA8761A	9	10	165	30	No	Yes
TDA8763A	10	10	175	30 (/3) 40 (/4) 50 (/5)	No	Yes
TDA8763	10	10	220	30 (/3) 40 (/4) 50 (/5)	Yes	Yes

The effective number of bits, when a full scale sine wave input is applied, stay above 9 bits for a 7.5 MHz signal frequency. Digitizing of full scale square wave signals (shape of CCD output signals) with the 10 bit resolution is possible if the settling time (typ 2,5 ns) and the input signal slope (max 400 V/ $\mu$ s) are respected.

The linearity performance of these ADCs ensures the 9 bit version the required conversion accuracy in case of 256QAM demodulator.

Because of their high analog bandwidth, a Sample & Hold is generally not required in front of the ADC analog input.

This ADC architecture allows a conversion time of only one clock cycle. In addition there is no restriction in using very low clock frequencies.

Application requires few external components and is similar for TDA8761A, TDA8763A and TDA8763. Except for the voltage references because the TDA8763 has integrated voltage references.

Consequently this note applies for the three converters (unless specified).

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TDA8763/61A/63A packages are a plastic shrink small outline package SSOP28 (SOT341-1).

The present demonstration board intends to facilitate an evaluation of the main TDA8763, TDA8763A, TDA8761A characteristics. It is realized with a three layers PCB with one internal ground plane. The following features are included :

- ⇒ On board quartz oscillator or a connection for an external clock. For ADC characteristic measurements a clock generator with a very low jitter should be used (see section 7).
- ⇒ ADC voltage references ( for A versions) and ADC 5V supplies are derived from a 8V supply by the means of voltage regulators.
- ⇒ Connectors allow external voltage references & external output supply (VCCO).
- ⇒ DC or AC input signals are allowed. The input offset can be provided in three different ways :
  - \* by a resistor bridge,
  - \* by a resistor connected to the middle reference voltage (pin 7),
  - \* by an external voltage source.
- ⇒ A 10 bits D/A converter has been added on the board to verify the proper operation of the ADC with an oscilloscope.

**The performances of the D/A converter are not as high as those of the A/D converter.** Consequently the on-board D/A converter can't be use for a correct study of the ADC characteristics.

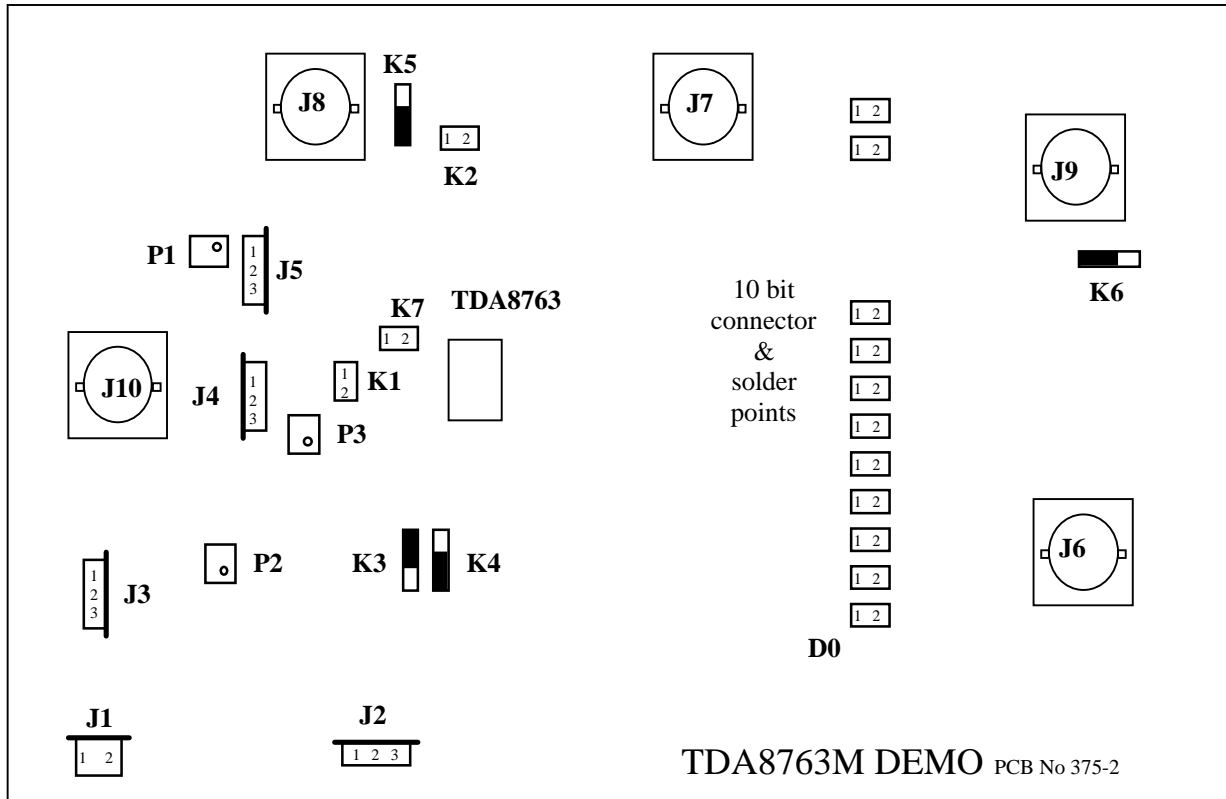
**WARNING :** The on-board D/A converter does not withstand a low output load, so it is necessary to check the strobe/scope input impedance before connection.

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## 2. CONNECTOR, SWITCH AND JUMPER POSITIONS





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### 3. CONNECTOR SWITCH AND JUMPER LIST

Reference	type	function
<b>J1</b>	2 point connector	<u>Board supply (8V)</u>
<b>J2</b>	3 point connector/jumper	<u>Internal/external VCCO supply selection</u> J2.1, Ground. J2.2,VCCO-ext: External input for VCCO. Must be connected with J2.3 if the internal VCCO is selected. An LC filter is provided between the J2.2 connector pin and the TDA8763M VCCO pin 13. J2.3, on board +5V for VCCO
<b>J3</b>	3 point connector/jumper	<u>Internal/external top reference selection:</u> J3.1, Ground J3.2, On-board adjustable top voltage reference J3.3, VTOP-ext: Pin for external top voltage reference connection, must be connected with J3.2 if internal top voltage reference is used.
<b>J4</b>	3 point connector/jumper	<u>Internal offset (provided by VMED)/external input offset selection</u> J4.1, Ground. J4.2, VMED: Vmedium voltage reference. Vmedium (tda8763 pin 7) can be use to provide input offset (If it is well decoupled from the input signal by a RC cell). In that case J4.3 and J4.2 must be connected. J4.3, IN-DC: This pin allows DC input connection or external input offset.
<b>J5</b>	3 point connector/jumper	<u>Internal/external bottom reference selection:</u> J5.1,VBOT-ext: Pin for external bottom voltage reference connection. J5.2,VBOT: Resistive load (1K potentiometer) must be connected with J5.1 if internal bottom voltage reference is used. J5.3,Ground
<b>J6</b>	BNC	<u>DAC output (high impedance probe is necessary)</u>
<b>J7</b>	BNC	<u>In range output (digital TTL output)</u>

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Reference	type	function
<b>J8</b>	BNC	<u>ADC (or ADC+DAC) clock input (50 <math>\Omega</math> input)</u>
<b>J9</b>	BNC	<u>DAC clock input (50 <math>\Omega</math> input)</u>
<b>J10</b>	BNC	<u>Signal input (50 <math>\Omega</math> input)</u>
<b>K1</b>	2 point jumper	<u>Internal offset (provided by a resistor bridge) connection</u> A resistor bridge (P3;R4;R9;C37) can be used to provide the input offset. In that case K1 must be connected. This resistor bridge is supplied by the top voltage reference.
<b>K2</b>	2 point jumper	<u>Clock test point</u>
<b>K3</b>	switch	<u>Two complement (pin 2) control</u> Upper position TC=1 (binary output) Lower position TC=0 (two complement output)
<b>K4</b>	switch	<u>Output Enable control (pin 10)</u> Upper position OE=1 (Output high impedance) Lower position OE=0 (output enabled)
<b>K5</b>	switch	<u>External/internal ADC clock selection</u> Lower position : internal clock selected Upper position : external clock selected (J8 connector)
<b>K6</b>	switch	<u>Internal/external clock selection for the DAC</u> Left position : internal clock selected Right position : external clock selected (J9 connector)
<b>K7</b>	2 point jumper	<u>Ground connection</u> Connected when testing TDA8761A or TDA8763A Not connected when testing TDA8763

#### **4. INITIAL SETTINGS: AC INPUT, ON BOARD QUARTZ OSCILLATOR, VOLTAGE REFERENCES**

The board supply must be set at 8 V.

All the supplies (ADC, DAC) are derived from a 7805 regulator and are well decoupled from each other by the means of LC filters. In this configuration the AC signal source must be provided by an external generator which is connected to the board by the J10 connector (dynamic input impedance is 50  $\Omega$ ).

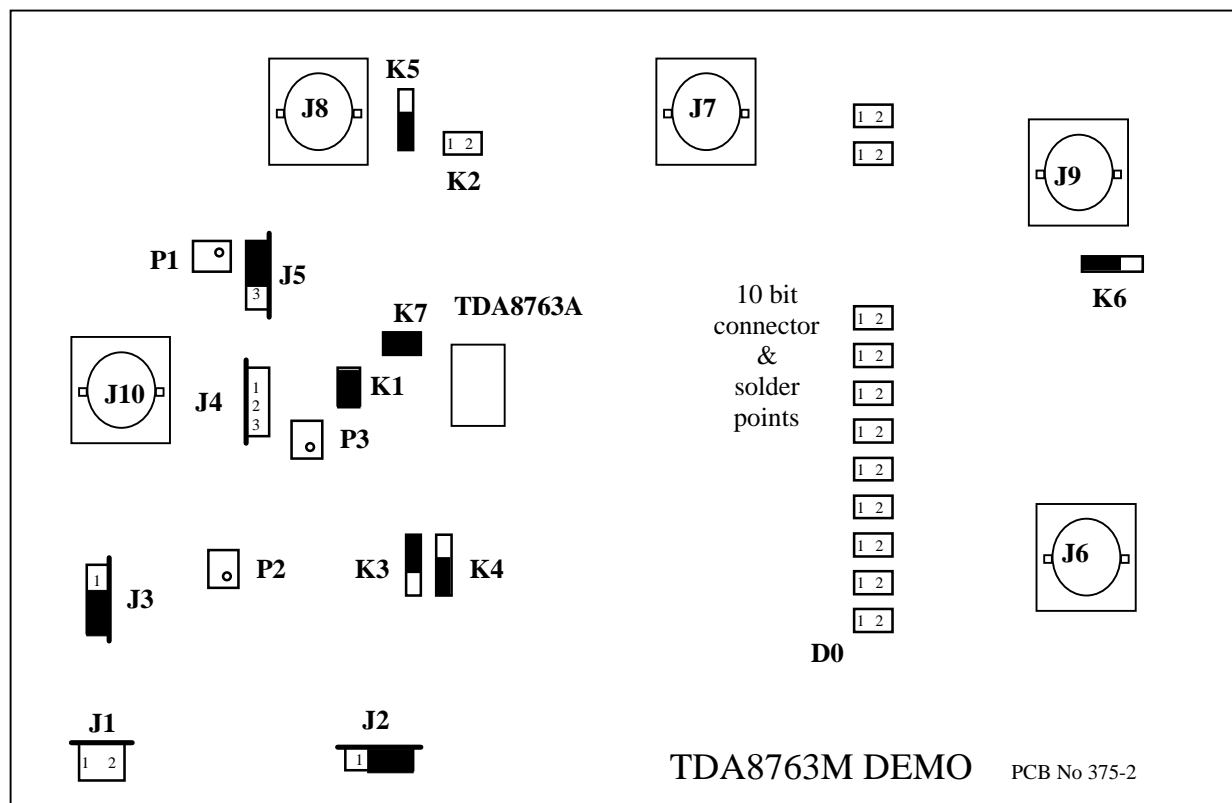
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The ADC top voltage reference is provided by an on-board adjustable regulator (TL431) and it is well decoupled by an LC filter. The ADC bottom voltage reference is simply set by a resistive load (P1 potentiometer). When a TDA8763 is used, top and bottom references are provided by the TDA8763 built-in voltage regulator, so the on-board references are no longer used, and the pin 5, 6 and 9 are decoupled to ground. The input offset is derived from the ADC top voltage reference and is made up of a resistor bridge (P3;R4;R9;C37).

To obtain this operational mode, jumpers, switches are set as shown in the following figure. When TDA8763 is used, **K7** and **J5** are **not connected** and the **L6** self is not soldered (see electrical diagram section 11).



Potentiometers P1, P2, P3 are adjusted as explained in the following :

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P2 is used to adjust the voltage of the on-board adjustable regulator (IC3). This regulator provides both: the ADC top voltage reference (for 'A' version) and the supply for the input offset (for all versions).

P2 is adjusted around:

175  $\Omega$  in order to obtain 3.43V at the adjustable regulator output for the TDA8761A

220  $\Omega$  in order to obtain 3.67V at the adjustable regulator output for the TDA8763A.

P1 allows the adjustment of the bottom voltage reference. In order to obtain a bottom reference of 1.3V, P1 is adjusted around:

150  $\Omega$  for the TDA8761A

134  $\Omega$  for the TDA8763A

(P1 is not used for the TDA8763)

P3 allows the adjustment of the input offset. In order to obtain an input offset around:

2.36V, P3 is adjusted around 2170 $\Omega$  for the TDA8761A

2.48V, P3 is adjusted around 2047 $\Omega$  for the TDA8763(A)

The dynamic input impedance at the analog signal input (J10 connector) is given by R9 (50 $\Omega$ ) and R4 (1K $\Omega$ ) in parallel and is equal to 48 $\Omega$ .

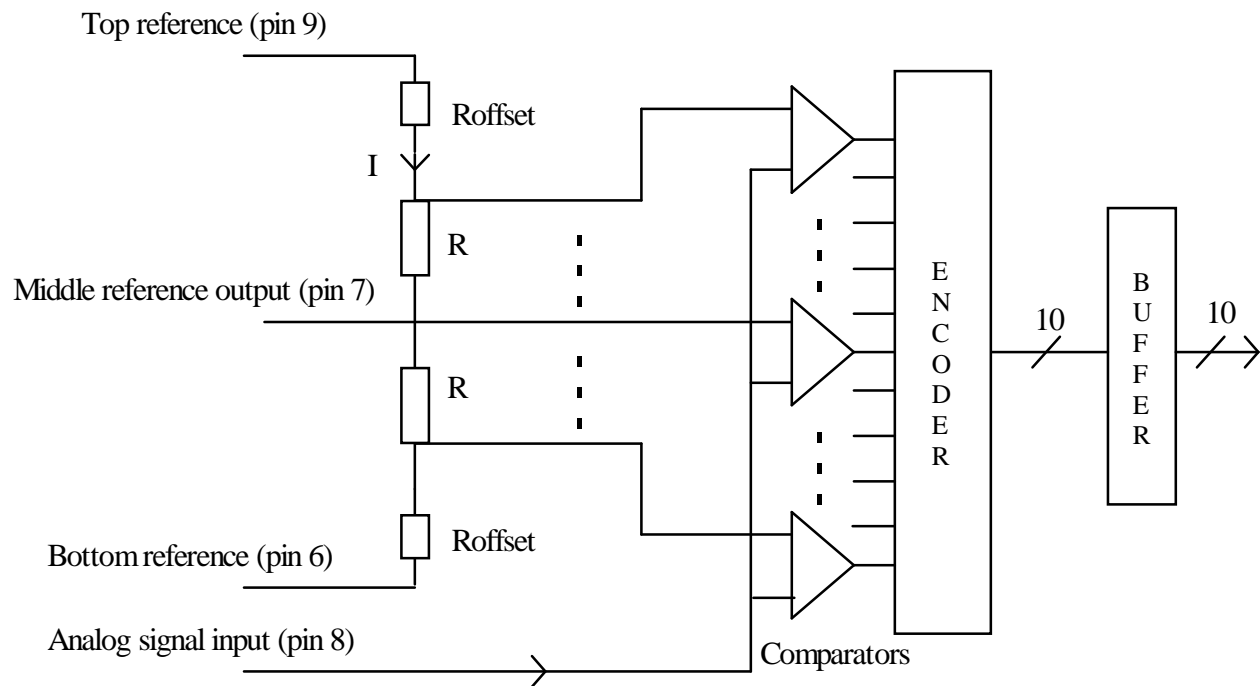
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## 5. VOLTAGE REFERENCES

Here is a block diagram which explains the TDA8763(A) working :



During the A to D conversion the analog input signal (pin 8) is compared to voltage references by using voltage comparators (In fact these comparators are folding amplifiers).

The full scale analog signal input range (FS) is given by:

$FS = 0.852 (V_{top} - V_{bottom})$ ; The 0.852 coefficient is due to the two offset resistors.

The comparator's voltage references are derived from a resistor ladder which is supplied through  $V_{top}$  (pin 9) and  $V_{bottom}$  (pin 6). Therefore if the  $V_{top}$  and  $V_{bottom}$  are not well regulated the A to D conversion will be affected. When using a TDA8763 the top and bottom references are provided by an on-chip regulator. In this case the top reference is fixed at 3.67V and the bottom reference is fixed at 1.3V (typical values).

Top reference (pin 9) is the highest voltage reference. Bottom reference (pin 6) is the lowest voltage reference. Consequently a current *I* is flowing from pin 9 to pin 6.

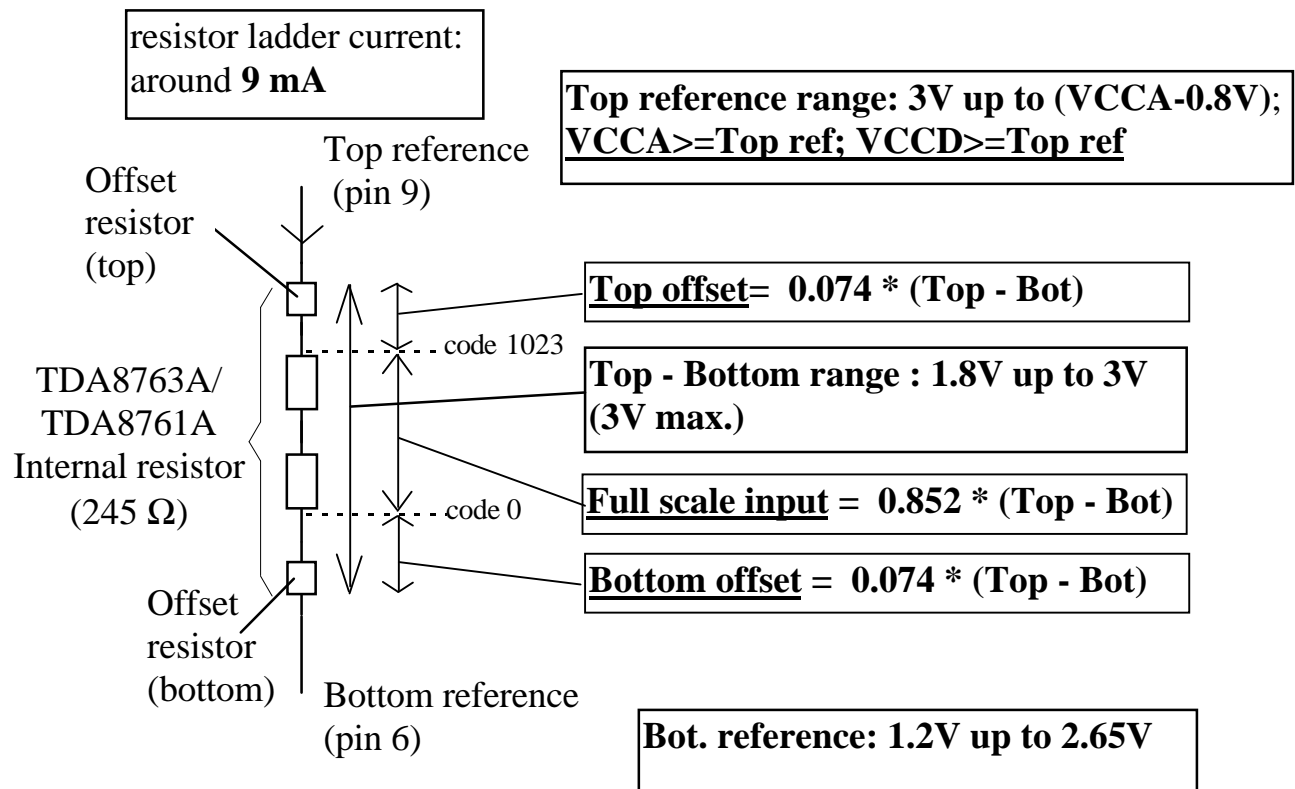
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The typical value for the internal resistor ladder is  $245\Omega$  at  $25^\circ\text{C}$ .

As shown in the following schematic the **TDA8763A** and **TDA8761A** are versatile regarding the choice of the top and bottom voltage references. Therefore it is possible to find top and bottom voltage references which fit with the majority



Concerning the **TDA8763**, because it has an integrated references regulator, top reference is fixed at 3.67V, bottom reference is fixed at 1.3V and the full-scale input is 2.02V. (typical values).

Note

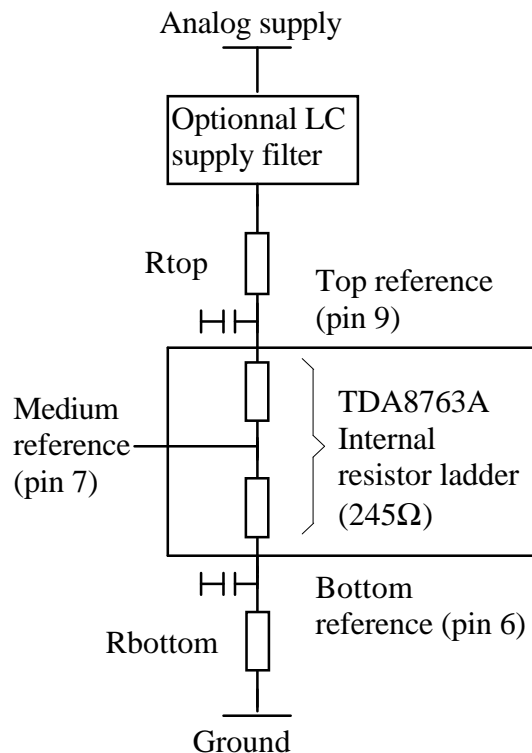
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Regulation of the  $V_{top}$  &  $V_{bottom}$  voltage references (**when using A versions**) depends on the level of cost and quality which are required by the customer application. Several methods providing these voltage references are shown in this section.

## 5.1 TOP & BOTTOM REFERENCES DERIVED FROM THE ANALOG SUPPLY

If the analog supply is well regulated a simple resistor bridge will be efficient (see following figure).



An optional filter can be added on the analog supply (depending on supply noise level).

Typical voltages for a 5V analog supply operation are 3.67V for top reference and 1.3V for bottom reference. The current flowing through the 245Ω resistor ladder is 9.6 mA ;

$$R_{top} = 137\Omega$$

$$R_{bot} = 134\Omega$$

Remarks: Here, the spreads due to process and temperature are not taken into account.

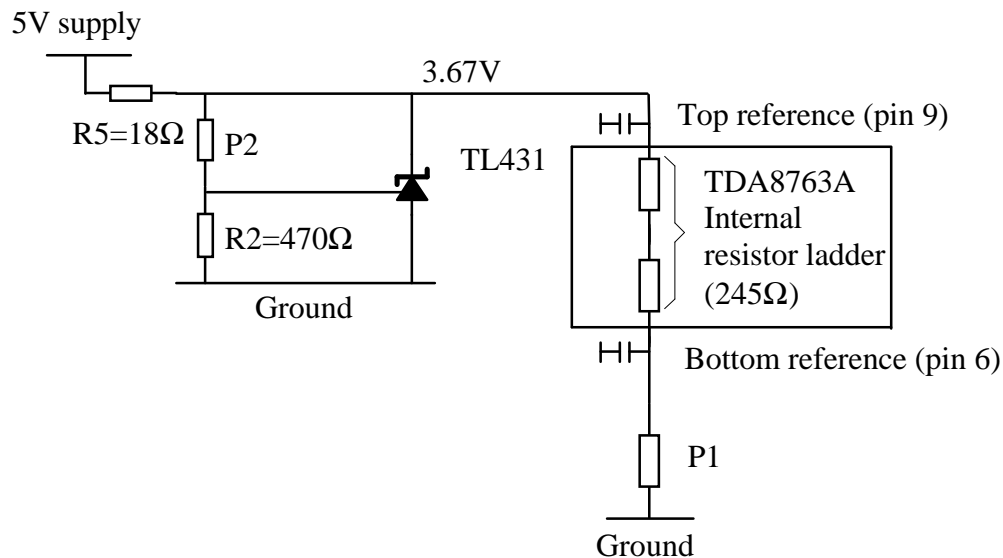
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## 5.2 TOP & BOTTOM REFERENCES DERIVED FROM VOLTAGE REGULATOR(S)

In some cases (noise on supply, several ADC's mounted in parallel ...) solutions with precision regulators (Philips  $\mu$ A723, Texas Inst. TL431,...) may be preferred. On this board a regulator (IC3, TL431) is used to provide the top reference whereas the bottom reference is simply made up of an adjustable resistive load (P1 potentiometer). It is possible to adjust, respectively, the top and bottom voltage value with the P2, and P1 potentiometers.



The voltage value of the top reference is given by the following formula :

$$V_{top} = 2,5 \left( 1 + \frac{P2}{R2} \right)$$

The voltage value of the bottom reference is given by :

$$V_{bot} = V_{top} \left( x \frac{R_{bot}}{R_{bot} + R_{ladder}} \right)$$

where  $R_{bot} = P1$  and  $R_{ladder}$  is the ADC internal ladder resistor (around  $245\Omega$ ).

It is also possible to connect external voltage references with two connectors, J3 (for the top reference) and J5 (for the bottom reference).

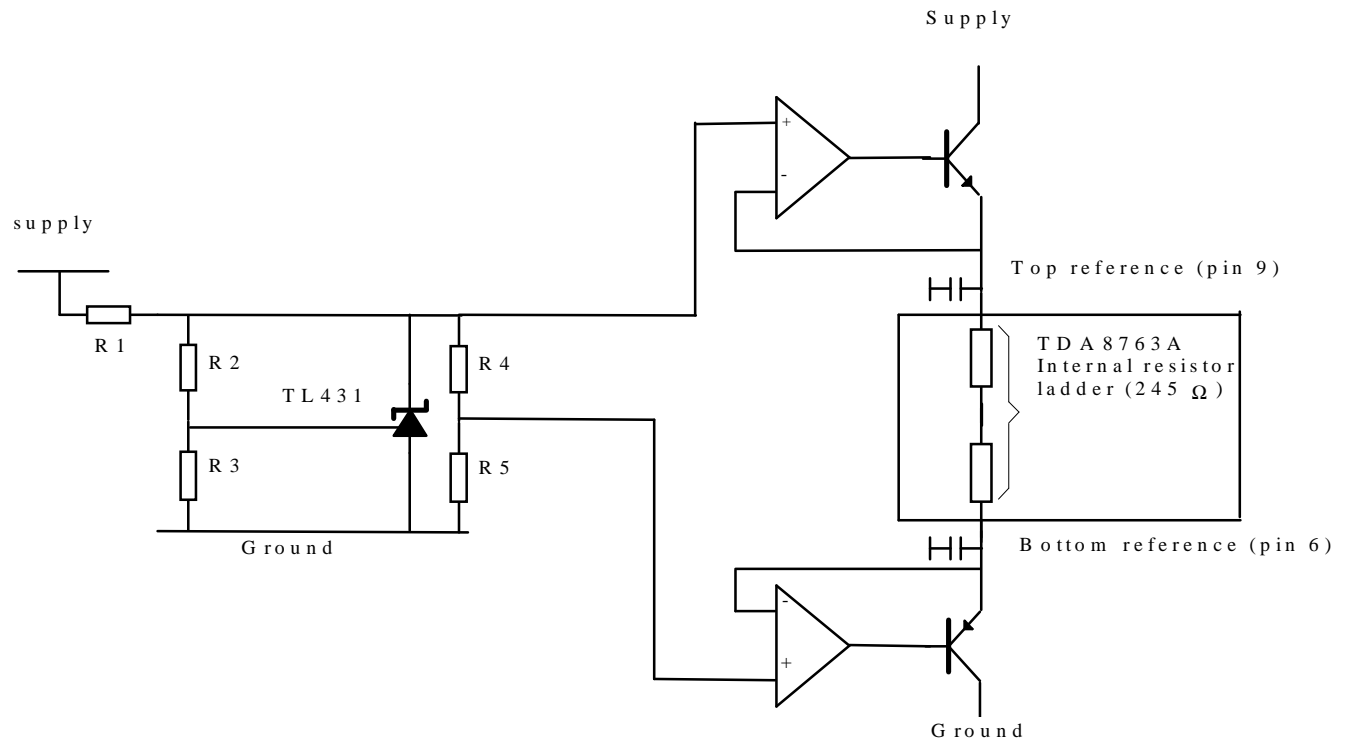


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If several ADC are mounted in parallel or if a very high precision of the voltage references over the whole temperature range is required, the following schematic can be used :



The transistor type depends on the number of TDA8763A mounted in parallel. A 9.5 mA current (typ) is required for each TDA8763A.

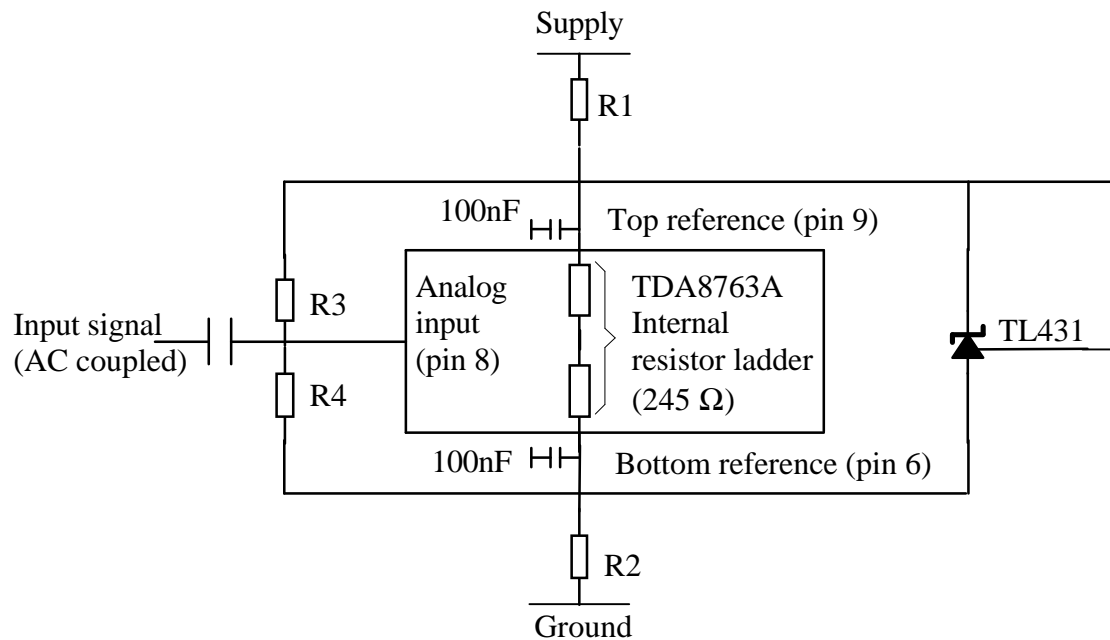
If only two or three ADC are used the operational amplifier and the transistor which drive the top reference can be skipped. In this case the external voltage regulator directly controls the top reference.

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In the following electrical diagram, top and bottom references are regulated by only one component (TL431):



The (top - bottom) difference is set at 2.5V by the TL431, so the full scale input is set at  $0.852 \cdot 2.5 = 2.13\text{V}$ . In addition the input offset is set at  $(V_{\text{top}} + V_{\text{bottom}})/2$  by two equal resistors (R3 and R4).

In this case the TL431 maintains the (top - bottom) difference at 2.5V over temperature and supply variations. Because the input offset is derived from the top and bottom references, it is also regulated at  $(V_{\text{top}} + V_{\text{bottom}})/2$  over the temperature and supply variations.

Using this method it is possible to drive the input offset and the top and bottom references of several TDA8763A with only one TL431.

Typical resistor values for a 5V application and for one TDA8763A are:

$R3 = R4 = 2.2\text{k}\Omega$ ,  $R1 = R2 = 25\Omega$ . The current flowing through the R1, R2 resistors is around 15 mA (The TL431 requires a minimum current to provide a proper regulation).

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## 6. INPUT OFFSET

When AC coupling is used with the TDA8763(A) it is necessary to provide an input offset in order to respect the TDA8763(A) full scale input range.

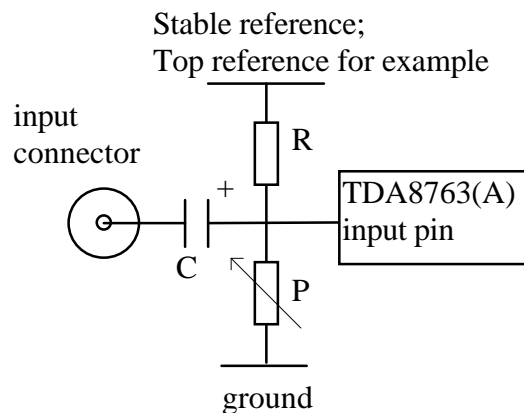
Relations between the  $V_{top}$  reference, the  $V_{bottom}$  reference, the maximum amplitude of the analog signal and the input offset are:

Max. amplitude of analog signal is  $(V_{top}-V_{bot}) \cdot 0.852$  and the input signal is centered around the input offset which is  $(V_{top}+V_{bottom})/2$ .

Consequently, if  $V_{top}=3.67V$  and if  $V_{bottom}=1.3V$  the maximum amplitude of the analog signal is 2.02V and the input offset is 2.48V; code 0 is obtained for a 1.475V input, and code 1023 is obtained for a 3.495V input.

Input offset can be provided by many different methods. Several methods are explained in this section.

### 6.1 INPUT OFFSET DERIVED FROM A RESISTOR BRIDGE



When a resistor bridge is used to provide an offset the current flowing through the resistors must be at least 10 times greater than the signal current (TDA8763(A) analog input current is 0 to 35 $\mu$ A) in order to guarantee the stability of the input offset. Consequently the resistive value of this resistor string must be below 10 K $\Omega$  (with a 3.67V top reference).

If the input signal generator used to test the TDA8763(A) requires a 50 $\Omega$  load, R must be set at 74 $\Omega$  and P at 154 $\Omega$  ( $V_{top}=3.67V$ ,  $V_{bottom}=1.3V$ , Input offset=2.48V), in order that the dynamic impedance (R & P in parallel) be 50 $\Omega$ .

Note

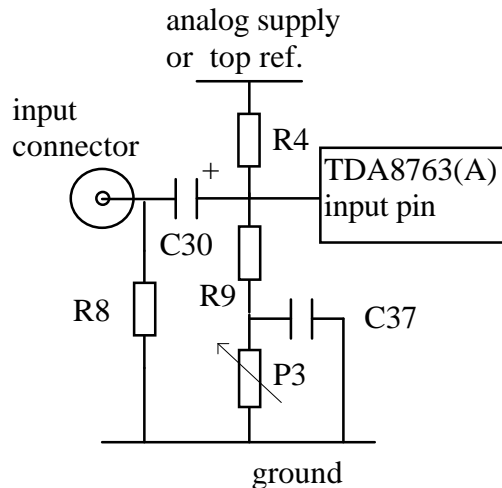
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Remarks:

This method provides a correct input offset but the current flowing through the resistor bridge is high: 16 mA ( $R=74\Omega$ ,  $P=154\Omega$  and top reference=3.67V).

In order to reduce this current consumption another method is used on board, but it requires two more components (one capacitor and one resistor):



R9 is equal to the output load of the external signal generator. C37 allows ground connection between R9 and P3 in dynamic mode. Typical values when a  $50\ \Omega$  signal generator is used are:  $R4=1\text{K}\Omega$ ,  $R9=50\Omega$ ,  $P3=5\text{K}\Omega$  (set at  $2047\Omega$ ),  $C37=10\text{nF}$ , then the current flowing through the resistor bridge is only 1.2 mA with a 3.67V supply. The solder print of an optional resistor R8 is provided in order to allow other impedance adaptations

- When it is possible, it is better to replace the potentiometers by fixed resistors. This will avoid possible distortion effects on the input signal due to the capacitive components of the potentiometers.
- It can be difficult to obtain the exact output load and the exact input offset when they are made up of fixed resistors, because the accuracy of the resistors is limited. Furthermore the resistor values change with temperature. Consequently in some professional applications it is better to provide the correct load and the correct input offset with operational amplifiers.

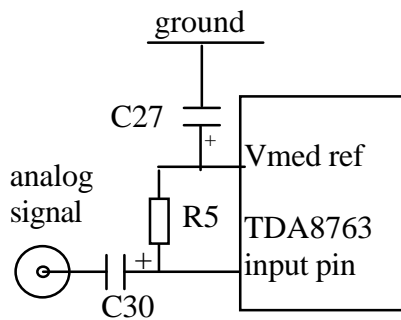
## 6.2 INPUT OFFSET DERIVED FROM THE MEDIUM REFERENCE

In this case the input pin is connected to the medium voltage reference (pin 7) with a resistor (R5). The medium voltage reference must be well decoupled by a capacitor (C27). The input impedance of the AD converter is given by R5 in parallel with  $Z_{in}$ .

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This method gives good results in the following domains: high common mode supply rejection (because both the voltage references and the input offset are derived from the same supply), very low noise level and low cost.

$R5 \cdot C27$  product must be high enough in order to avoid a coupling between the input signal and the medium reference.

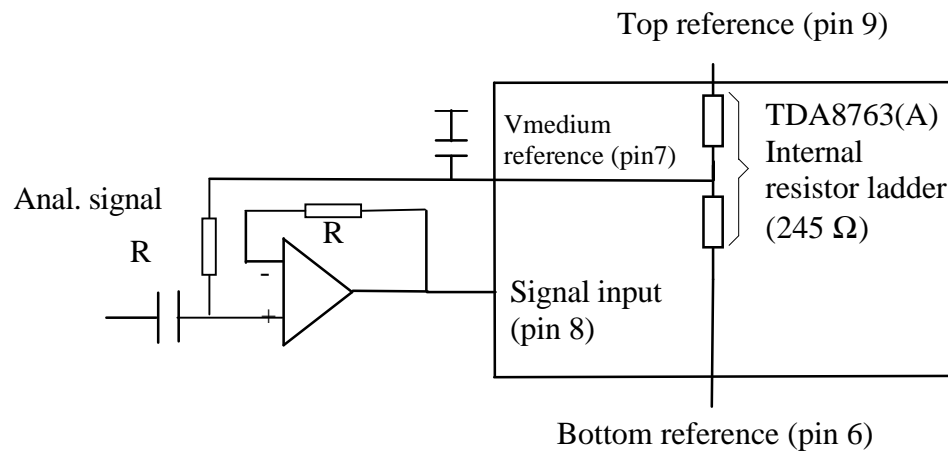
( $C27=4.7\mu\text{F}$  for example) The offset on the input pin is:  $V_{\text{med}} - (35\mu\text{A} \cdot R5)$ .

On board selection of the input offset, provided by the medium reference, is allowed by the J4.3 & J4.2 connection. In this case R5 and C27 must be soldered (SMD 1206 series solder prints).

### 6.3 INPUT OFFSET PROVIDED BY AN OPERATIONAL AMPLIFIER

The middle output reference voltage and a low input offset operational amplifier can be used to provide an accurate input offset. Several methods can be used :

1°)



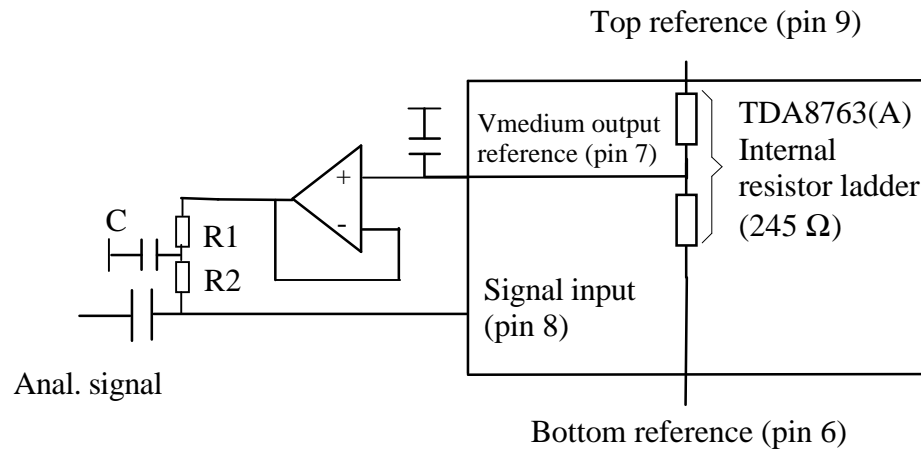
The R resistor in the op-amp loop compensates the offset due to the R resistor connected to  $V_{\text{med}}$ . ( $R=1\text{k}\Omega$ ;  $C=1\mu\text{F}$ )

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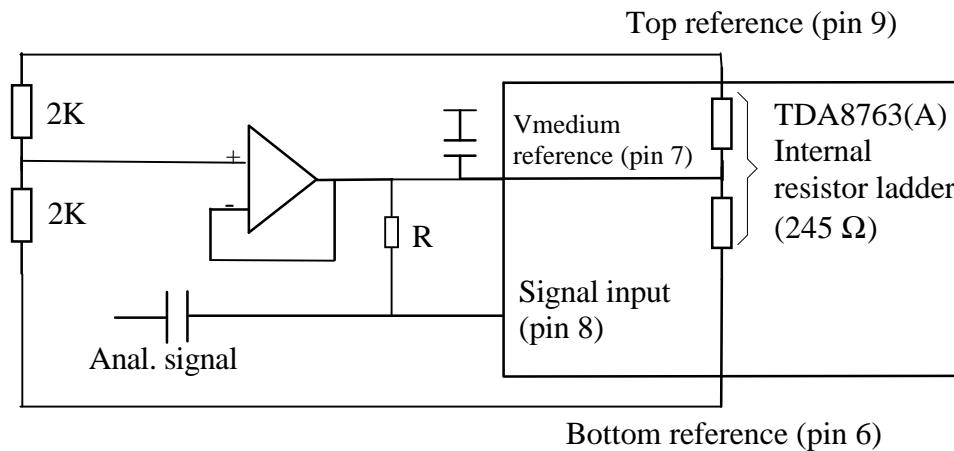
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2°)



The amplifier does not need a high bandwidth, but the necessary time to load the C capacitor at 'power on' depends on the op.amp maximum output current. The input impedance is  $R2 // Zin$ .  $Zin$  is the ADC input impedance.

3°)



Medium reference is derived from top and bottom reference (input impedance is  $R // Zin$ ).

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## 7. CLOCK

### 7.1 CLOCK INPUT

The TDA8763(A) clock input (pin 1) is made up of a long pair tail ; therefore a low level AC clock input is allowed.

The clock input threshold is fixed at  $V_{CCD}/2V$ . Consequently the DC component of the clock must be adjusted around 2.5V.

Also, the threshold value makes the TDA8763(A) clock input compatible with CMOS levels.

### 7.2 CLOCK JITTER

If the clock jitter and the slope of the analog input signal are high, sampling errors can appear.

Example:

The equation of a sinewave signal is  $s(t)=A/2 \sin(2 \pi F t)$ ,

where **A** is the ADC full scale amplitude (**A=1024 LSB**) and **F** is the sinewave frequency.

The slope of this signal is given by:

$$ds(t)/dt=A/2 2 \pi F \cos(2 \pi F t)$$

this slope is maximum when  $t=0$  (input voltage level is around middle code 511/512):

$$ds(0)/dt=A \pi F \text{ Volt/second.}$$

That means that the middle code is available at the ADC input only during:

$$T_{lsb}=LSB/(A \pi F)=(1024 \pi F)^{-1} \text{ second.}$$

If the full scale sinewave frequency is **F = 10 Mhz**, then **T<sub>lsb</sub> = 31 ps**

Consequently the clock jitter must be lower than this value.

If a 20 Mhz full scale sinewave is sampling, the jitter must be lower than 15 ps.

#### Remarks :

If the sample clock frequency and the input signal frequency have the same jitter (or phase noise), the sampling error due to jitter can be avoided.

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Consequently it is not suitable to do precise dynamic measurements of the ADC characteristics with the on board quartz oscillator, except if the input signal frequency and the quartz oscillator frequency are correlated.

## **8. ADC SUPPLIES**

All the ADC supplies VCCA (pin 3), VCCD2 (pin 11), VCCO (pin 13), VCCD1 (pin 28) are derived from the on board 7805 regulator and are well decoupled from each others by the means of LC filters.

VCCA stands for TDA8763(A) analog parts supply.

VCCD1, VCCD2, stand for TDA8763(A) digital internal digital supplies.

VCCO stands for TDA8763(A) digital output buffer supply.

Generally all the supplies are fixed around 5V and the differences between supplies must stay in the range of -0.2V to +0.2V. (-0.2V to +2.25V for VCCA-VCCO and VCCD-VCCO).

VCCO can be adjusted down to 3V.

In some cases (low voltage logic output interface, see section 9) it may be interesting to decrease the value of VCCO. This is allowed on the demo-board with the J2 connector.

## **9. DIGITAL OUTPUTS / LOW VOLTAGE LOGIC COMPATIBILITY**

The TDA8763(A) digital outputs have a CMOS structure.

The maximum digital high output level of the TDA8763(A) is always lower than the outputs supply VCCO.

In addition, the VCCO supply is adjustable from 5.25V down to 3V, so the maximum digital high output level can be reduced to the low voltage supply level.

This will ensure the compatibility between the TDA8763(A) outputs and the low voltage logic inputs.

For general information about 3V and 5V logic compatibility refer to the AN240 application note included in the IC23 Philips databook.



Note

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## **10. 10 BIT D/A CONVERTER**

A 10 bit 5V supply/TTL input DAC (IC1) allows **rough** ADC evaluation with a scope or a spectrum analyzer. Analog output level is in the range of 3 to 5 volts.

**The performances of the D/A converter are not as high as those of the A/D converter.** Consequently the on-board D/A converter cannot be use for a correct study of the ADC characteristics.

### **WARNING:**

This D/A converter does not support low output loads, so it is necessary to check the strobe/scope input impedance before connection to the load.

## **11. DEMO BOARD DOCUMENTATION : ELECTRIC DIAGRAM, COMPONENT LIST & COMPONENT PLACE**

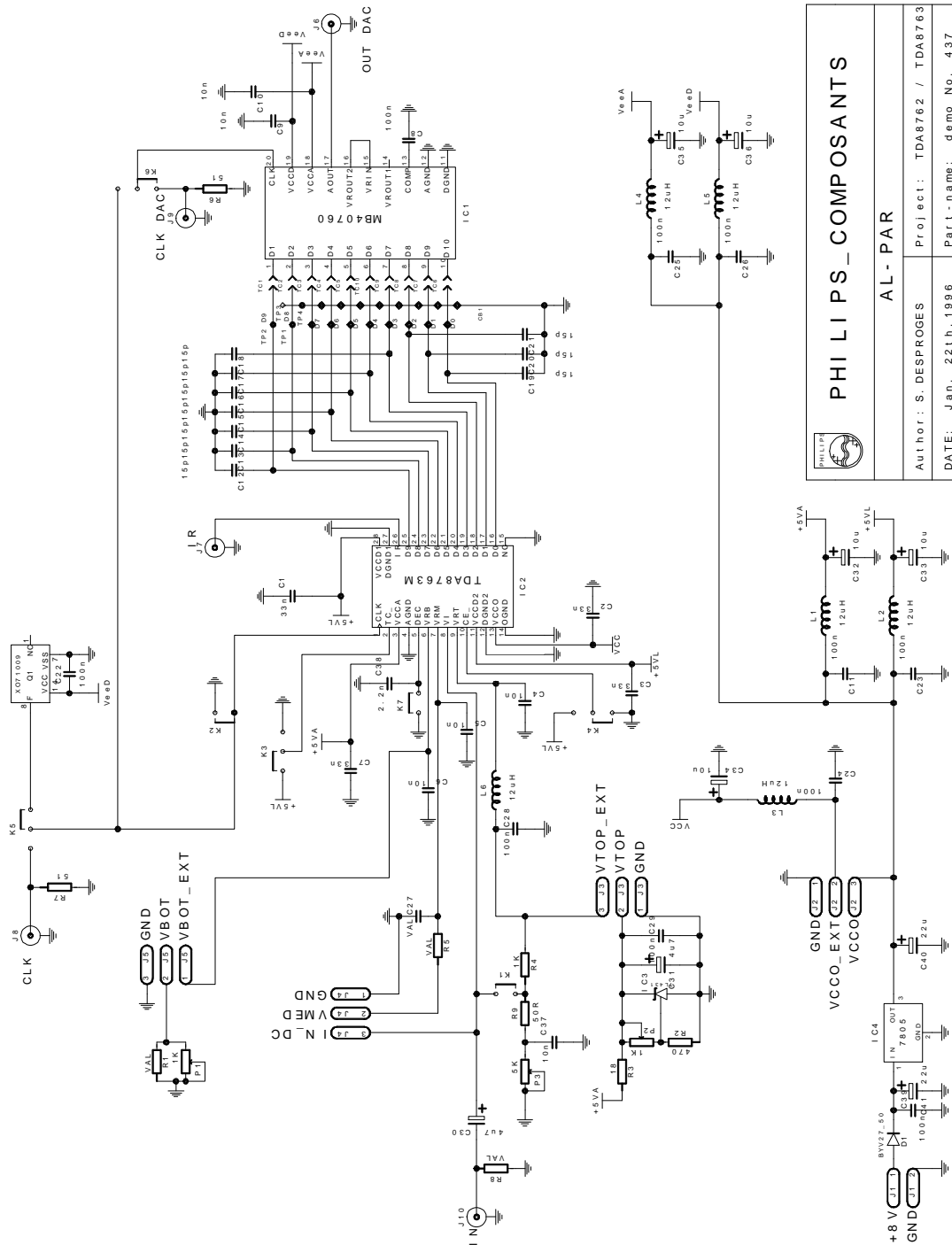
### **11.1 ELECTRIC DIAGRAM**

(see next page)

Note

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<b>PHILIPS COMPONENTS</b>	
AL - PAR	
Author: S. DESPROGES	Project: TDA8762 / TDA8763
DATE: Jan. 22th, 1996	Part - name: demo No. 437

Note

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## 11.2 COMPONENT LIST

Reference	Value	Component
C1	33N	C0805
C2	33N	C0805
C3	33N	C0805
C4	10N	C0805
C5	10N	C0805
C6	10N	C0805
C7	33N	C0805
C8	100N	C1206
C9	10N	C1206
C10	10N	C1206
C11	100N	C1206
C12	15P	C1206
C13	15P	C1206
C14	15P	C1206
C15	15P	C1206
C16	15P	C1206
C17	15P	C1206
C18	15P	C1206
C19	15P	C1206
C20	15P	C1206
C21	15P	C1206
C22	100N	C1206
C23	100N	C1206
C24	100N	C1206
C25	100N	C1206
C26	100N	C1206
C27	VAL	C1206
C28	100N	C1206
C29	100N	C1206
C30	4 $\mu$ 7	SPRAGUE_595D_A

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Reference	Value	Component
C31	4 $\mu$ 7	SPRAGUE_595D_A
C32	22 $\mu$	SPRAGUE_293D_D
C33	22 $\mu$	SPRAGUE_293D_D
C34	22 $\mu$	SPRAGUE_293D_D
C35	22 $\mu$	SPRAGUE_293D_D
C36	22 $\mu$	SPRAGUE_293D_D
C37	10N	C0805
C38	2.2N	C0805
C39	100N	C1206
C40	22 $\mu$	SPRAGUE_293D_D
C41	22 $\mu$	SPRAGUE_293D_D
CB1		8 BITS CONNECTOR (LSBs)
D1		BYV27_50
IC1		MB40760
IC2		TDA8762T
IC3		TL431
J1		CONN353MV2
J2		CONN1X3V_FCON
J3		CONN1X3V_FCON
J4		CONN1X3V_FCON
J5		CONN1X3V_FCON
J6		BNC
J7		BNC
J8		BNC
J9		BNC
J10		BNC
K1		2 POINT JUMPER
K2		2 POINT JUMPER
K3		SWITCH
K4		SWITCH
K5		SWITCH
K6		SWITCH
K7		2 POINT JUMPER
L1	12 $\mu$ H	LQH4N

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<b>Reference</b>	<b>Value</b>	<b>Component</b>
L2	12 $\mu$ H	LQH4N
L3	12 $\mu$ H	LQH4N
L4	12 $\mu$ H	LQH4N
L5	12 $\mu$ H	LQH4N
L6	12 $\mu$ H	LQH4N
P1	1K	3224W
P2	1K	3224W
P3	5K	3224W
Q1	20 up to 50MHz	X071009
R1	Optional	RMR01
R2	470	RMR01
R3	18	RMR01
R4	1K	RMR01
R5	VAL	RMR01
R6	51	RMR01
R7	51	RMR01
R8	VAL	RMR01
R9	50	RMR01
TC1-TC10		SOLDER POINTS
TP1-TP4		Test points 2 bits connector (MSBs)

Note

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11.3 COMPONENT PLACE

